What is claimed is:

1. A test circuit for a logical integrated circuit, comprising:

plural flip-flops of a scanning type (FFs, hereinafter) arranged in first to n th stages, in each of which said FFs are successively connected in series,

plural logic gates, output terminals of which are respectively connected with input terminals of said plural FFs, and

a scan path which is formed of a series connection of a part or a whole of said plural FFs, and propagates a test pattern for measuring an alternating current (AC, hereinafter) characteristic of an input or output terminal of said logical integrated circuit,

wherein said scan path connects an output terminal of said FF standing at an end of said first stage with a scan output.

2. A test circuit for logical integrated circuit, comprising:

plural FFs arranged in first to n th stages, in each of which said FFs are successively connected in series,

plural logic gates, output terminals of which are respectively connected with input terminals of said plural FFs, and

a scan path which is formed of a series connection of a part or a whole of said plural FFs, and propagates a test pattern for measuring an AC characteristic of an input or output terminal of said logical integrated circuit,

wherein said scan path connects a scan input with an input terminal of said FF standing at a head of said n th stage.

3. A test circuit for a logical integrated circuit, comprising,

plural FFs arranged in first to n th stages, in each of which said FFs are successively connected in series,

plural logic gates, output terminals of which are respectively connected with input terminals of said plural FFs, and

a scan path which is formed of a series connection of a part or a whole of said plural FFs, and propagates a test pattern for measuring an AC characteristic of an input or output terminal of said logical integrated circuits,

wherein said scan path connects a scan input with an input terminal of said FF standing at a head of said n th stage,

again successively connects said FFs arranged in said second to (n-1) th stages in series, after restarting from an output terminal of said FF standing at an end of said n th stage,

once again connects an output terminal of said FF standing at an end of said (n-1) th stage with an input terminal of said FF standing at a head of said first stage, and

finally connects an output terminal of said FF standing at an end of said first stage with a scan output.

4. A method for testing a logical integrated circuit, which is compose of:

plural FFs arranged in first to n th stages, in each of which

said FFs are successively connected in series,

plural logic gates, output terminals of which are respectively connected with input terminals of said plural FFs, and

a scan path which is formed of a series connection of a part or a whole of said plural FFs, and propagates a test pattern for measuring an AC characteristic of an input or output terminal of said logical integrated circuit, comprising the steps of:

connecting an output terminal of said FF standing at an end of said first stage with a scan output,

inputting a clock signal to a clock signal input terminal,

inputting a predetermined data signal to one of said input terminals of said logical integrated circuit, and

measuring said AC characteristic of said one of said input terminals of said logical integrated circuit by inspecting an output of said scan output.

5. A method for testing a logical integrated circuit, which is composed of:

plural FFs arranged in first to n th stages, in each of which said FFs are successively connected in series,

plural logic gates, output terminals of which are respectively connected with input terminals of said plural FFs, and

a scan path which is formed of a series connection of a part or a whole of said plural FFs, and propagates a test pattern for measuring an AC characteristic of an input or output terminal of said logical integrated circuit, comprising the steps of:

connecting a scan input with an input terminal of said FF standing at a head of said n th stage,

inputting a clock signal to a clock signal input terminal,

inputting a predetermined data signal to a scan input, and

measuring an AC characteristic of one of said output terminals of said logical integrated circuit by inspecting an output of said one of said output terminals.

6. A method for testing a logical integrated circuit, which is composed of:

plural FFs arranged in first to n th stages, in each of which said FFs are successively connected in series,

plural logic gates, output terminals of which are respectively connected with input terminals of said plural FFs, and

a scan path which is formed of a series connection of a part or a whole of said plural FFs, and propagates a test pattern for measuring an AC characteristic of an input or output terminal of said logical integrated circuit, comprising the steps of:

connecting a scan input with an input terminal of said FF standing a head of said n th stage,

connecting said FFs arranged in said second to (n-1) th stages successively in series, after restarting from an output terminal of said FF standing at an end of said n th stage,

connecting an output terminal of said FF standing at an end of said (n-1) th stage with an input terminal of said FF standing at a head of said first stage,

connecting an output terminal of said FF standing at an end

of said first stage with a scan output,

inputting a clock signal to a clock signal input terminal,

inputting a predetermined data signal to one of said input terminals of said logical integrated circuit, and

measuring said AC characteristic of said one of said input terminals of said logical integrated circuit by inspecting an output of said scan output.

7. A method for testing a logical integrated circuit, which is composed of:

plural FFs arranged in first to n th stages, in each of which said FFs are successively connected in series,

plural logic gates, output terminals of which are respectively connected with input terminals of said plural FFs, and

a scan path which is formed of a series connection of a part or a whole of said plural FFs, and propagates a test pattern for measuring an AC characteristic of an input or output terminal of said logical integrated circuit, comprising the steps of:

connecting a scan input with an input terminal of said FF standing a head of said n th stage,

connecting said FFs arranged in said second to (n-1) th stages successively in series, after restarting from an output terminal of said FF standing at an end of said n th stage,

connecting an output terminal of said FF standing at an end of said (n-1) th stage with an input terminal of said FF standing at a head of said first stage,

connecting an output terminal of said FF standing at an end

of said first stage with a scan output,

inputting a clock signal to a clock signal input terminal,

inputting a predetermined data signal to a scan input, and

measuring an AC characteristic of one of said output terminals of said logical integrated circuit by inspecting an output of said one of said output terminals.